

This data sheet provides specifications for the 2109E, 2113E, and 2117F computers. All specifications apply to each of these computers, unless otherwise noted. Product descriptions and ordering information can be found in the individual product data sheets.

M-Series data sheets are located in the Mature Products section of this data book. The 2111F computer will not be available after mid-1982, and its data sheet has been omitted from this data book. For information concerning the 2111F, please retain your previous HP 1000 Hardware data book.

Functional specifications

Processor architecture

Implementation: Microprogrammed in MSI and SSI hardware

Data path width: 16 bits

Standard registers:

Accumulators: 2 (A and B), 16 bits each, addressable as registers or memory locations

Index: 2 (X and Y), 16 bits each

Memory control: 3 (T,P) 16 bits each; (M), 15 bits

Supplementary: 2 (overflow and extend), 1 bit each

Manual data: 16-bit (display)

Instruction types:

Memory-to-accumulator Accumulator-to-I/O

Memory-to-memory Device control

Direct register modification

Instruction expansion: 176 instruction codes are available to the microprogrammer for instruction set additions.

Addressing modes:

Direct Double word

Multi-level indirect Single word

Indexed Byte

Indirect indexed Bit

Register implicit

Bus structure: Separate memory data, memory address, and I/O buses tied to the unified internal S Bus

Memory structure: 32 pages of 2048 bytes, with direct access to current or base page (page 0) pages; indirect or indexed access to all pages

Memory expansion: Paged memory address space expandable to 1024 pages of 2048 bytes using the Dynamic Mapping System

Input/Output: Vectored priority interrupt structure for up to four system devices and 46 I/O devices, such as DCPC, power fail, parity, and memory protect.

Control processor

Implementation: Hardwired MSI and SSI TTL

Instruction execution time: Variable, 175 or 280 nsec

Control path: 24 bits

Data path: 16 bits

Registers:

Standard registers: 6 (A,B,X,Y,P,S)

Scratch registers: 12 16-bit registers accessible to the microprogrammer

Iteration counter: 8 bits

Instruction register: 16 bits

Latch register: 16 bits

Status flag: 1 bit

Subroutine levels stack: 3 - 14 bits each

Instruction formats:

TYPE 1 Data transfer and modification

TYPE 2 Constant formation

TYPE 3 Conditional branch

TYPE 4 Unconditional branch

Bus structure: Unified single bus with program access to memory data, memory address, and I/O buses.

Bus speed: 11.4M bytes/sec.

Control memory structure:

Type: Bipolar LSI semiconductor R/W or ROM

Address space: 16,384 words; 64 modules of 256-words each

Word size: 24 bits

Cycle time: Variable, 175 or 280 nsec

Module assignments

F-Series:

(1 module = 256 words of control memory)

0 - 3 assigned to F-Series base instruction set, including Floating Point Processor instructions.

4 - 11 Reserved for HP enhancements.

12 - 15 Reserved for Vector Instruction Set.

16 - 17 Reserved for HP enhancements.

18 - 27 RTE-6/VM Operating System instructions.

28 - 31 Available for user microroutines.

32 Reserved for Dynamic Mapping Instructions.

33 - 35 Reserved for Fast FORTRAN Processor.

36 & 37 Reserved for RTE-IVB Extended Memory Area (EMA) or RTE-6/VM EMA/VMA mapping instructions.

38 & 39 Reserved for DS/1000 firmware.

40 - 43 Reserved for Scientific Instruction Set.

44 & 45 Reserved for HP enhancements.

46 - 63 Available for user microroutines.

E-Series:

- (1 module = 256 words of control memory)
- 0 - 3 Assigned to E-Series base instruction set
- 4 - 31 Available for user microroutines
- 32 Reserved for DMS instructions
- 33 - 35 Reserved for Fast FORTRAN Processor
- 36 & 37 Reserved for RTE-IVB Extended Memory Area (EMA) or RTE-6/VM EMA/VMA mapping instructions
- 38 & 39 Reserved for DS/1000 firmware
- 40 - 43 Reserved for future HP instruction set enhancements
- 44 & 45 RTE-6/VM Operating System instructions
- 46 - 63 Reserved for user microroutines

Control processor instructions: 211 total; up to 5 may be combined in 1 instruction.

E/F-Series:

- Operations: 15 total.
- Special: 32 total.
- ALU and conditional: 68 total.
- Store (destination): 32 total.
- S-bus (source): 32 total.
- Reverse Sense: 32 total.

Loader protection

All loaders reside in special ROM's on the CPU board. The loader routines are assembly code routines which are loaded into the last 64 words of main memory by activating front panel switches. Four switch-selectable loader spaces are provided to accommodate four different loader routines. User-generated loaders may be written in assembly language, written into PROMS, and mounted in any of the four available sockets on the CPU board.

Volatility protection

AC standby mode and sustaining power for line loss of 8 milliseconds before entering power fail routine. Power fail recovery system provides a minimum of 1.6 hours of battery-supplied memory standby power.

Memory parity check

Monitors all words read from memory. Utilizes 17th bit in memory. Switch programmable to halt, interrupt, or ignore parity error when detected. Interrupt on error requires memory protect option. Indication of a parity error is displayed by a light on the front panel.

Approximate instruction execution times for E/F-Series Computers

Instruction	Execution Time (μsec) in F-Series
Single-precision Floating Point (32 bit) Instructions (8 total)	
Add/Subtract	7.7
Multiply	6.4
Divide	9.3
Conversion to single integer	5.3
Conversion to double integer	6.3
Conversion from single integer	4.6
Conversion from double integer	5.7
Extended-precision Floating Point (48 bit) Instructions (8 total)	
Add/Subtract	13.8
Multiply	13.0
Divide	17.4
Conversion to single integer	6.8
Conversion to double integer	8.7
Conversion from single integer	6.6
Conversion from double integer	8.1
Double-precision Floating Point (64 bit) Instructions (8 total)	
Add/subtract	14.9
Multiply	13.7
Divide	19.7
Conversion to single integer	7.3
Conversion to double integer	9.2
Conversion from single integer	7.0
Conversion from double integer	8.5
Single-Precision (32 bit) Scientific Instruction Set Instructions (9 total)	
SIN (Sine) function	51.8
COS (Cosine) function	52.0
TAN (Tangent) function	53.7
ATAN (Arc Tangent) function	52.6
TANH (Hyperbolic Tangent) function	66.5
SQRT (Square Root) function	37.8
EXP (e _x) function	51.9
ALOG (Natural Logarithm) function	46.3
ALOGT (Base 10 Logarithm) function	52.6
Double-Precision (64 bit) Scientific Instruction Set Functions♦	
SIN (Sine) function	217.0
COS (Cosine) function	217.0
TAN (Tangent) function	212.0
ATAN (Arc Tangent) function	189.0
TANH (Hyperbolic Tangent) function	211.0
EXP (e _x) function	219.0
SQRT (Square Root) function	135.0
ALOG (Natural Logarithm) function	179.0
ALOGT (Base 10 Logarithm) function	214.0

♦The double-precision Scientific Instruction Set functions are a combination of firmware (approximately 90%) and software (approximately 10%); the software is included in the relocatable libraries of all compatible RTE operating systems.

Fault control memory and dynamic mapping system may each add 0 to 0.2 microsecond to these instruction execution times.

Asynchronous memory may cause variations of ±0.035 microseconds per memory reference.

More detailed instruction times are supplied in the HP 1000 F-Series reference manual (02111-90001).

The maximum non-interruptible time for any instruction is 12.2 milliseconds.

All execution times are worst case figures.